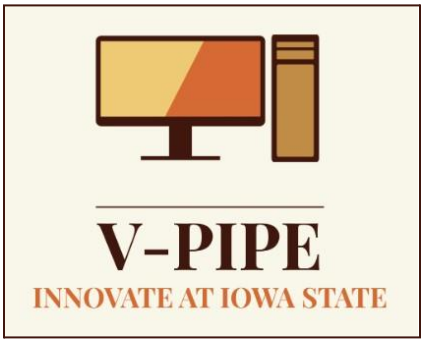


EE/CprE/SE 4920 WEEKLY REPORT 1

08/26/2024 – 09/05/2024
Group number: 6
Project title: Video Pipeline for Machine Vision
Client: JR Spidell
Advisor: Dr. Phillip Jones

Team Members: Ritwesh Kumar (Video Stream to FPGA), Deniz Tazegul (Video Stream to FPGA), Liam Janda (VDMA to DDRM), Taylor Johnson (DDRM to Displayport)

o Weekly Summary

This week, the team met with the client to brainstorm theories and plans for action to prove or disprove ideas to get a TPG image to send to the VDMA with the desired resolution, pattern, and synchronization. The team discovered that setting the VDMA FSYNC mode to TUSER and the TPG max data width parameter to 8 bits in Vivado provided the expected resolution and synchronization, however, the TPG pattern had a different color output than expected.

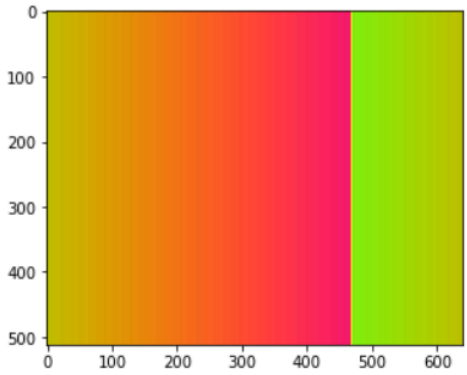
o Past week accomplishments

- **Deniz:** Caught up with the team to see what progress was made over the summer, saw presentations and the current state of the code base. Started looking at the TPG datasheet to come up with some theories to test.
- **Liam:** Liam caught Deniz up on the progress that was made over the summer, including going over the presentations and our current program. Presented what was odd and unexpected about our current frame outputs, as well as our current known unknowns. Met with Ritwesh and Taylor to run tests using the overlays and TPG patterns provided to us.
- **Taylor:** Worked with Ritwesh to run tests with our code. The focus was on buffer allocation and experimenting with flushing and invalidating the buffers. The results were added to the team's slide deck documenting our debugging process. While running various tests, Taylor and Ritwesh dug into the overlay and printed out the information for the TPG. Experimented with changing different TPG background patterns to see how that impacted the results after updates to the TPG were made in Vivado and updated the team's slide deck.

- **Ritwesh:** Met with Deniz to help explain the team's progress over the summer. Ritwesh worked on updating the team's pipeline configuration slideshow for documenting potential theories to help understand and ultimately, helped fix the synchronization errors including end-of-line (EOL) late and start-of-frame (SOF) late errors that happened due to incorrect TPG and VDMA settings in Vivado. Ritwesh also met with Taylor and Liam to run tests in a Jupyter Notebook to see how different Vivado configurations impacted the data sent by the TPG to the VDMA in terms of expected resolution, synchronization, and color output while keeping the underlying PYNQ code constant.

o **Pending issues**

Currently, the team is experiencing issues with getting the proper colors to appear. For example, when the TPG's background pattern is set to solid red, it is seen as blue. The team is observing a noticeable shift in the pattern for certain TPG patterns such as color sweep (shown below).



- **Deniz:** None.
- **Liam:** None.
- **Taylor:** None.
- **Ritwesh:** None.

o **Individual contributions**

Name	Individual Contributions	Hours this week	Cumulative Hours
Deniz	Caught up with the team and began looking at the TPG datasheet.	3	3
Liam	Catching Deniz up on the project, presenting what was odd/unexpected about our VDMA frames, as well as our current known unknowns. VDMA research.	6	6
Taylor	Ran various tests to gather information for proving/disproving the team's theories to explain what we observed in our TPG_VDMA code and documented the results in the team's slide deck.	7	7
Ritwesh	Worked on updating the team's pipeline configuration slides to document changes to the code and results, and helped fix the synchronization issues (end-of-line late and start-of-frame late errors) between the TPG and VDMA.	10	10

o **Plans for the upcoming week**

- **Deniz:** Work with the team on TPG issues and creating the MIPI start-up script in PYNQ.
- **Liam:** Continue to work with the team to come up with potential theories as to why our VDMA frames are not what they should be. Look into why the VDMA does not write to the Ultra96 DDR memory.
- **Taylor:** Continue to work on debugging the TPG. Try to determine why the colors are not what the team expects.

- **Ritwesh:** Continue brainstorming theories and testing new Vivado configurations to fix the incorrect color output sent by the TPG.

Action Item	Task Owner	Expected Date
Schedule a time to meet with the team's advisor	All	09/06/2024
Figure out what is causing the TPG cross-hatch pattern to have an uneven spacing of horizontal and vertical lines	All	09/19/2024

o **Summary of weekly advisor meeting**

The team has not had a meeting with the advisor yet, but has contacted him and will have a meeting as soon as possible.